54. (Amended) The multi-die module as in Claim 58, wherein the packaged semiconductor die is a memory.

## REMARKS

Applicants have requested the cancellation of claims 1, 15, 43 and 49 without prejudice Further, Applicants have presented new claims 56 – 59, and accordingly, request a new prior art search. Applicants have also submitted amendments to claims 2-6, 8, 9, 11, 16-18, 20, 23, 44-47, 53 and 54. In addition, Applicants submit that the new language in the new claims and in the amended claims do not include new matter.

**Fallon et al.**

Previously, the Examiner alleged that Fallon et al. disclosed an unpackaged semiconductor die, (864; FIG. 46), encapsulated, (876; FIG. 46), in encapsulation material. Applicants submit that, more specifically, Fallon et al. discloses such encapsulated material as only having an arc, or dome shape and is also shown to rise to a height that is approximately half the height of a neighboring package module. (FIG. 46). This is unlike Applicants' claimed subject matter having, inter alia, an "encapsulated ... structure having a planar top surface ... wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate. (claim 56).

Further, Applicants submit that the encapsulation design of Fallon et al. lacks the advantages present in Applicants' claimed subject matter. For example, Applicants' planar top surface of an encapsulation structure which is positioned in a coplanar fashion relative to the top portion of a neighboring package module, such that a heat sink having a planar bottom (e.g., a simple universal design), can be placed on top of both the top surface of the encapsulation structure and the top portion of a neighboring package module such that the heat sink is in contact with both items and rests upon a relatively large portion of both items where the large

contact, between both the encapsulation structure and the neighboring package module and the heat sink, allow for significant heat transfer from both items to the heat sink. In contrast, the encapsulation design disclosed in Fallon et al. is less desirable than Applicants' claimed subject matter because when a heat sink, having a planar surface, is placed on top of both the packaged and encapsulated semiconductor dies, such heat sink then assumes an angled position across the two items. In such a position the heat sink only contacts the edge of the packaged heat sink and only a point of the dome of the encapsulated material. As such, thus resulting in a heat transference is relatively small and the physical connection to the heat sink is positioned on an undesirable angle resulting in a number of disadvantages. It should be also noted that, regardless of the height of the top surface of the domed shaped encapsulated structure, any heat sink with a planar surface in contact with that domed shape only shares a small contact position therewith, and as such, will result in a relatively poor transference of heat therebetween.

Also previously, the Examiner alleged that Fallon et al. disclosed an encapsulating structure, (876; FIG 46), comprised of an encapsulating material including a metal cap. (col. 37, ln. 64). Applicants submit that such encapsulating material is disclosed by Fallon et al. as only being organic material. (id.) This is unlike Applicants' claimed subject matter having, inter alia, an "encapsulating structure ... further comprised of an encapsulating material of a metal cap." (claim 59).

Further, Applicants submit that the encapsulation design of Fallon et al. lacks the advantages present in Applicants' claimed subject matter. An example of such an advantage includes the fact that Applicants metal cap encapsulation technique provides the advantages associated with the properties of metallic structures generally, and more specifically, for some embodiments, the presence of a gap between the enclosed die and surrounding metal cap

structure itself. In contrast, the organic encapsulation material design disclosed in Fallon et al. is less desirable than Applicants' claimed subject matter as such material is not metal and therefore does not provide the metallic properties provided by Applicants' claimed subject matter, nor is such material a metal cap that, in some embodiments, allow for a void between the enclosed die and the surrounding structure.

**New Claims**

Independent Claim 56

Independent claim 56 is a new claim and recites, among other features, ... an ... unpackaged semiconductor die encapsulated onto the package module in a structure having a planar top surface; and a packaged semiconductor die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

Applicants respectfully reassert the arguments made above regarding Fallon et al. Applicants submit that, Fallon et al. does not disclose, teach or suggest, claim 56's language including, inter alia, "...an ... unpackaged semiconductor die encapsulated onto the package module in a structure having a planar top surface; and a packaged semiconductor die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate," nor does Fallon et al. disclose, teach or suggest the subject matter of claim 56 as a whole. Applicants submit that at least for the reasons that Fallon et al. discloses an encapsulated structure with only a dome shaped top surface, and where such domed shaped top surface is described as being located at a position that is only half the height of a neighboring

package module, that independent claim 56 is neither anticipated, nor is obvious in view of Fallon et al.

Independent Claim 57

Independent claim 57 recites, among other features, ... a ... graphics-processing die encapsulated on the package module in a structure having a planar top surface; and a packaged memory die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the substrate.

Applicants respectfully reassert the arguments made above regarding Fallon et al. Further, Applicants submit that, Fallon et al. does not disclose, teach or suggest, claim 57's language including, inter alia, "...a ... graphics-processing die encapsulated on the package module in a structure having a planar top surface; and a packaged memory die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the substrate.," nor does Fallon et al. disclose, teach or suggest the subject matter of claim 57 as a whole. Applicants submit that at least for the reasons that Fallon et al. discloses an encapsulated structure with only a dome shaped top surface, and where such domed shaped top surface is described as being located at a position that is only half the height of a neighboring package module, that independent claim 57 is neither anticipated, nor is obvious in view of Fallon et al.

Independent Claim 58

Independent claim 58 recites, among other features, an unpackaged semiconductor die ... encapsulated in a structure having a planar top surface; and a packaged semiconductor die having a top surface and mounted on the first surface of the substrate; wherein the planar top surface of

the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

Applicants respectfully reassert the arguments made above regarding Fallon et al. Further, Applicants submit that, Fallon et al. does not disclose, teach or suggest, claim 58's language including, inter alia, "...an unpackaged semiconductor die ... encapsulated in a structure having a planar top surface; and a packaged semiconductor die having a top surface and mounted on the first surface of the substrate; wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.," nor does Fallon et al. disclose, teach or suggest the subject matter of claim 58 as a whole. Applicants submit that at least for the reasons that Fallon et al. discloses an encapsulated structure with only a dome shaped top surface, and where such domed shaped top surface is described as being located at a position that is only half the height of a neighboring package module, that independent claim 58 is neither anticipated, nor is obvious in view of Fallon et al.

Independent Claim 59

Independent claim 59 recites, among other features, an unpackaged semiconductor die ... encapsulated in a structure; and a packaged semiconductor die mounted on the first surface of the substrate wherein the encapsulating structure is further comprised of an encapsulating material of a metal cap.

Further, Applicants submit that, Fallon et al. does not disclose, teach or suggest, claim 59's language including, inter alia, "...an unpackaged semiconductor die ... encapsulated in a structure; and a packaged semiconductor die mounted on the first surface of the substrate wherein the encapsulating structure is further comprised of an encapsulating material of a metal cap," nor does Fallon et al. disclose, teach or suggest the subject matter of claim 59 as a whole.

Applicants submit that at least for the reasons that Fallon et al. discloses an encapsulated structure limited to organic material, that independent claim 59 is neither anticipated, nor is obvious in view of Fallon et al.

**Amended Claims**

Claims 2-6, 8, 9, 11, 16-18, 20, 23, 44-47, 53 and 54 have been amended to more accurately claim the subject matter that Applicants regard as the invention. Further, Applicants submit that since each amended claim depends from one of the new claims identified above, that such dependent claims are allowable, at least for the reasons discussed above as to why the corresponding independent claim is allowable.

Attached hereto, on an attached page labeled "Version with Markings to Show Changes Made," is a marked-up version of the changes made to the claims in the current Amendment.

Applicants respectfully submit that the claims are in condition for allowance. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

By: _____
Brent A. Boyd
Reg. No. 51,020

Dated: February 13, 2003

Vedder, Price, Kaufman & Kammholz
222 North LaSalle Street
Chicago, Illinois 60601
Telephone: (312) 609-7500
Facsimile: (312) 609-5005

## Version with Markings to Show Changes Made

**In the claims:**

2. (Amended) The device as in Claim [1] 56, wherein the packaged semiconductor is packaged in a ball grid array package.

3. (Amended) The device as in Claim [1] 56, wherein the unpackaged semiconductor die is a graphics-processor.

4. (Amended) The device as in Claim [1] 56, wherein the packaged semiconductor is a memory.

5. (Twice Amended) The device as in Claim [1] 56, wherein a plurality of packaged semiconductors are attached to the package module.

6. (Twice Amended) The device as in Claim [1] 56, wherein the unpackaged semiconductor die is wire bonded to the package module.

8. (Amended) The device as in Claim [1] 56, wherein attached includes surface-mount technology reflow.

9. (Thrice Amended) The device as in Claim [1] 56, wherein the encapsulated structure has a footprint greater than the footprint of the unpackaged semiconductor die.

11. (Amended) The device as in Claim [1] 56, wherein the footprint size of the package module is one of 35mm X 35mm, 31mm X 31mm, 27mm X 27mm, 37.5mm X 37.5mm, 40mm X 40mm, 42mm X 42mm, or 42.5mm X 42.5mm.

16. (Amended) The device as in Claim [1] 56, wherein the packaged memory is packaged in a ball grid array package.

17. (Twice Amended) The device as in Claim [15] 57, wherein a plurality of packaged memory are attached to the package module.

18. (Twice Amended) The device as in Claim [15] 57, wherein directly attached includes the graphics processing die being wire bonded to the package module.

20. (Amended) The device as in Claim [15] 57, wherein attached includes surface-mount technology reflow.

23. (Amended) The device as in Claim [15] 57, wherein the standard package sizes include one of 35mm X 35mm, 31mm X 31mm, 27mm X 27mm, 37.5mm X 37.5mm, 40mm X 40mm, 42mm X 42mm, or 42.5mm X 42.5mm.

44. (Amended) The multi-die module as in Claim [43] 58, further including a second packaged semiconductor die mounted on the first surface of the substrate.

45. (Amended) The multi-die module as in Claim [43] 58, further including a plurality of unpackaged semiconductor die mounted on the first surface of the substrate.

46. (Amended) The multi-die module as in Claim [43] 58, wherein the unpackaged semiconductor die is mounted to the first surface of the substrate by wire bonding.

47. (Amended) The multi-die module as in Claim [43] 58, wherein the encapsulating structure is further comprised of an encapsulating material including epoxy, metal cap or silicon coatings.

53. (Amended) The multi-die module as in Claim [43] 58, wherein the unpackaged semiconductor die is a graphics processor.

54. (Amended) The multi-die module as in Claim [43] 58, wherein the packaged semiconductor die is a memory.

56. (New) A device comprising:

a package module including a substrate having a standard package footprint;

an unpackaged semiconductor die directly attached to the package module, the unpackaged semiconductor die encapsulated onto the package module in a structure having a planar top surface; and

a packaged semiconductor die having a top surface and attached to the package module;

wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

57. (New) A device comprising:

a package module sized to be interchangeable with standard package sizes;

a graphics-processing die directly attached to the package module, the graphics-processing die encapsulated on the package module in a structure having a planar top surface; and

a packaged memory die having a top surface and attached to the package module;

wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the package module.

58. (New) A multi-die module, comprising:

a substrate having a first surface and a second surface;

an unpackaged semiconductor die mounted to the first surface of the substrate, the semiconductor die encapsulated in a structure having a planar top surface; and

a packaged semiconductor die having a top surface and mounted on the first surface of the substrate;

wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

59. (New) A multi-die module, comprising:

a substrate having a first surface;

an unpackaged semiconductor die mounted to the first surface of the substrate, the semiconductor die encapsulated in a structure; and

a packaged semiconductor die mounted on the first surface of the substrate wherein the encapsulating structure is further comprised of an encapsulating material of a metal cap.